Ultra-Low Loss SiN Edge Coupler for III-V/SiN Hybrid Integration

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Silicon photonics is becoming a competitive technology to settle the issues of power and speed in data centers and computing systems. However, the absence of an on-chip light source restricts the wide and deep application of silicon photonics. Essentially, efficient edge coupling from a Si-based III-V laser to silicon photonic components remains the major obstacle for on-chip integration. Here, two compact edge couplers with ultra-low coupling loss and eased fabrication for the light transmission from a Si-based III-V laser to Si_3N_4 waveguide are realized. An ultra-low laser-to-chip coupling loss of only 1.175 dB for the butt coupling of a Si-based InAs QD laser is experimentally demonstrated with high alignment tolerance. The strategies presented here provide a competitive solution for realizing ultra-efficient integration of Si-based light sources and silicon photonic components.

1. Introduction

Due to the explosive growth of data centers and cloud computing, the requirement for high-performance and high-density optical interconnect is dramatically increasing. Silicon photonics (SiPh) is appearing as a strongly competitive solution for the increasingly severe communication bottleneck of power and speed faced by conventional electrical interconnects.[1,2] SiPh has been fascinating tremendous research interest due to the CMOS process compatibility, low cost, and high integration density.[3–5] Silicon (Si) and silicon nitride (Si_3N_4) are the primary materials for the multitudinous SiPh devices. Si possesses the aptitude for high-speed modulation and large-scale high-density integration,[1,6] while Si_3N_4 is superior in passive devices due to the wide working bandwidth, high nonlinearity, and extremely low propagation loss.[7,8] Numerous SiPh devices with various functions have been presented, such as modulators,[9,10] filters,[11,12] (de)multiplexer [13,14] and optical frequency comb.[15,16] These devices have been widely applied in various research fields such as optical interconnect,[17] optical telecommunication,[18] light detection and ranging (LiDAR) [19] and microwave photonics.[20] Some devices have even been initially commercialized, such as III-V/Si laser[21] and 800 Gbps transmitters.[22]

However, limited by the indirect bandgap essence of Si or Si_3N_4 material, reliable, high-yield, and low-cost monolithic Si-based light sources for SiPh are not yet available. The integration of III-V lasers with SiPh is a crucial step toward widespread application. Achieving efficient on-chip lasers has always been the grail for SiPh. Although III-V active components can be bonded to Si-on-Insulator (SOI) and Si_3N_4-on-Insulator (SiNOI) wafers through wafer bonding strategy, where light couples to the underlying waveguide evanescently, there are still troubles of cost and thermal dissipation.[23] Alternatively, III-V material directly grown on Si substrates has got high potential to be a more economical and favorable solution, which not only eliminates the necessary for expensive III-V wafers and the complex bonding process but also possesses extra merits of compact packaging and excellent heat dissipation.[24,25] The monolithic Si-based laser is identified as one of the most prospective methods for future complete integration.[23,26–28]

Nevertheless, a major challenge for Si-based lasers is the efficient light coupling to Si/Si_3N_4 waveguide. A feasible solution is a hybrid integration using butt coupling between an external Si-based laser and a passive SiPh platform.[29,30] Hybrid integration is a straightforward and easily implemented method. The III-V light sources and the passive Si/Si_3N_4 devices can be optimized and fabricated on different wafers to achieve their best performance separately and then integrated together through butt coupling strategy. Moreover, it is more convenient to manage the heat dissipation on the separated active and passive chips. Butt coupling an external cavity laser (ECL) has been becoming an essential scheme in optical systems for the superiorities such as narrow linewidth and high wavelength tunability. Plenty of latest research concentrates on ECLs for further improvements in their output power,[31] linewidth, [32] and tuning range.[33]

In the present butt coupling schemes, due to the absence of high-efficiency edge coupler, a momentous matter is the huge

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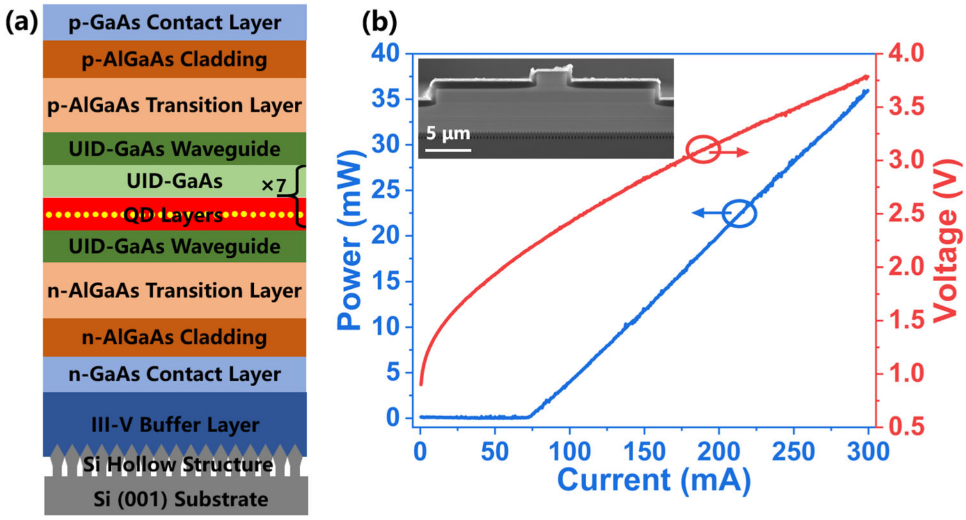

Figure 1. a) Structure of the InAs/GaAs QD laser directly grown on Si [001] substrate. b) Typical *L–I–V* performance of the laser with size of 4 μm × 2000 μm. The inset is the cross-sectional SEM picture of the Si-based laser.

mismatch of mode field distribution between III-V laser and passive Si/Si_3N_4 chip, causing the large coupling loss (commonly >3 dB), which degrades the performance of the elaborately designed passive devices and hinders their application. Fortunately, SiNOI platform possesses not only low waveguide propagation loss but also low refractive index contrast, which avails the butt coupling between the III-V laser and the Si_3N_4 photonics platform, thereby ensuring splendid laser performances.

In this paper, we thoroughly analyze and experimentally realize an efficient butt coupling from epitaxial Si-based laser to SiNOI platform. The InAs/GaAs quantum dot (QD) laser is directly grown on a Si substrate. With only a 100 μm coupling length, an ultra-low light coupling loss of 1.175 dB with a large alignment tolerance for Si_3N_4 chip is obtained. To the best of our knowledge, this is the best butt coupling efficiency for the III-V/SiN hybrid integration. The Si-based laser has a threshold current of 75 mA and a slope efficiency of 0.16 W A^{-1}. The maximum output power is 36 mW. This ultra-low loss butt coupling of Si-based laser and SiNOI chip provides a feasible and promising strategy for complete SiPh integration with both active and passive components.

2. Si-based QD Laser

The O-band InAs/GaAs QD laser is directly grown on a Si [001] substrate. First, U-shaped grating structures along the [110] direction are fabricated on a Si [001] substrate. Then the patterned substrate is put into the SiGe molecular beam epitaxy (MBE) chamber for homoepitaxial growth of Si buffer layers with sawtooth hollow structures [111]. As shown in **Figure 1**a, the sawtooth-structured hollow Si substrate is then transferred to the III-V MBE chamber for in situ heteroepitaxial growth of III-V buffer layers and InAs/GaAs QD laser structures. The growth details can be found in ref. [26, 28]. The [111]-faceted sawtooth structures can annihilate antiphase boundaries effectively and eliminate most of dislocations induced by the lattice mismatch at III-V/Si interface, while the thermal stress can be relieved effectually utilizing the hollow structures. The detailed fabrication information is shown in Section S5 (Supporting Information).

The Si-based InAs/GaAs QD narrow ridge Fabry-Perot laser is then fabricated from the materials prepared above with standard laser fabrication processes. The inset in Figure 1b shows the cross-sectional SEM image of an as-cleaved Si-based ridge laser with a size of 4 μm × 2000 μm, indicating a mirror-like cavity facet. The fabricated Si-based laser is then attached to an aluminum nitride chip carrier, which is fixed on the top of a thermoelectric cooler (TEC) with silver epoxy. The temperature of TEC is set at 23 °C during measurement. The continuous-wave (CW) light–current–voltage (*L–I–V*) property is measured to study the laser performance with the device dimension of 4 μm × 2000 μm. As shown in Figure 1b, the threshold current of the QD laser is 75 mA. The measured 1.6 V turn-on voltage from the *I–V* curve indicates good metal contacts of the laser diode and a resistance of 8 Ω of the device can be extracted. Above the threshold, the output power follows a kink-free curve, indicating excellent mode stability. The slope efficiency is ≈0.16 W A^{-1}, and a maximum output power of 36 mW can be obtained from the Si-based laser at an injection current of 300 mA.

3. Ultra-Low Loss Si_3N_4 Edge Couplers

In butt coupling strategy, difficulty and complexity in fabrication and packaging are the inescapable challenges. Employing the multilayers [34–36] or suspended schemes [37–39] can distinctly improve the coupling efficiency. However, in a standard photonics foundry, enormous challenges will be generated in the fabrication and packaging due to the excrescent complexity and difficulty. Excellent coupling performance can also be achieved by appending intermediate polymer material,[40,41] but limited to the physical boundedness of the material itself, such as reliability, robustness, scalability, etc., this scheme has not achieved extensive application. In our previous work, edge couplers with a simplified fabrication process are demonstrated, which is an essential step forward toward efficient coupling between fiber and SOI chip on a large scale.[42,43] Inspired by the imperious requirement of integrated photonics and based on our accumulation on light coupling, we propose ultra-low loss Si_3N_4 edge couplers for Si-based laser and SiNOI chip. In this edge coupler design, only a single layer and planar structure are needed, therefore just one lithography and etching process is required. This design tremendously simplifies the fabrication and furnishes great feasibility and repeatability.

The proposed edge couplers for the butt coupling between Si-based laser and SiNOI chip are shown in **Figure 2**. The couplers are fork shape structures, which can efficiently couple light from laser to Si_3N_4 waveguide. To acquire high coupling efficiency, the mode field at the SiNOI chip facet must spatially overlap the laser mode field to the greatest extent (Section S1, Supporting Information). As illustrated in Figure 2a, when light transmits from a laser to a chip through an edge coupler, the laser mode preferentially contacts with SiNOI chip facet with a double-tip, which produces a large modal overlap. Then the light is transferred into the slot waveguide adiabatically and finally transferred into a 1.5 µm wide strip waveguide through the 100 µm long coupler.

As shown in Figure 2b,c, three fundamental parameters of fork1 coupler during fabrication, the tip width (w), tip gap (g), and coupler length (L), are optimized by the Lumerical 3D-FDTD simulation at 1310 nm. For tip width, the optimal coupling loss is 1.04 dB at 210 nm [Figure 2e], which can be directly fabricated using the conventional CMOS process. The optimal tip gap is 1.8 µm with a coupling loss of 1.05 dB. The coupling is almost stable when the coupler length is >80 µm, and an optimum value, 100 µm, is chosen in the fabrication. It is worth mentioning that this fork structure shows strong fabrication tolerance. In the range from 150 nm to 250 nm of tip width, the coupling losses are all smaller than 1.15 dB. Similarly, the tip gap ranges from 1 µm to 2.5 µm, variation of the loss is only 0.15 dB. In Figure 2h, the black solid and dashed lines demonstrate the fork1 coupler performance in the O band, for this simple and straightforward structure, a portion of the input TE0 light will transfer into other modes in the coupling process. So the losses of coupled light, which contains total modes and only TE0 mode, are analyzed. For the total mode, the monitor collects all the energy of every mode, the coupling loss maintains smaller than 1.1 dB in 100 nm wavelength range. For the TE0 mode, the monitor collects the energy of only TE0 mode, the coupling loss is 1.23 dB at 1310 nm, which is 0.2 dB higher than the total mode loss.

To improve the coupled mode purity of TE0 mode, an additional 40 µm adiabatic coupling part is added to fork2 coupler. Through the adiabatic transformer, light undergoes single-mode conditions, and the inter-modal cross-coupling along the device is negligible.[44–46] The analogous optimization of structure parameters for fork2 coupler is presented in Section S2 (Supporting Information), the total length of fork2 coupler is 100 µm, and two parameters, the optimal tip width is 180 nm and the tip gap is set as 1.2 µm. In Figure 2h, the red solid and dashed lines denote the coupling loss of fork2 coupler. At 1310 nm, the deviation of loss between total modes and TE0 mode is only 0.01 dB, meaning an extremely high mode purity.

The proposed edge couplers are fabricated on a SiNOI wafer, the thickness of top Si_3N_4 device layer is 200 nm, and the buried oxide layer is 3 µm thick. Benefiting from the simplified structure, the coupler is defined just through a single electron beam lithography process. The resist pattern is fully etched using the Inductively Coupled Plasma-Reactive Ion Etching etching process in the device layer. Subsequently, after removing the photoresist, a 3 µm thick SiO_2 cladding layer is deposited using a plasma-enhanced chemical vapor deposition process. A deep etching process is employed to get a smooth edge facet. Finally, the integral chip is diced into several separate chips for measurement. The detailed fabrication information is shown in Section S4 (Supporting Information). The optical and SEM pictures of the fabricated edge couplers are shown in Figure 2i,j.

4. Ultra-Low Loss Butt Coupling for III-V/SiN Hybrid Integration

Figure 3 demonstrates the measurement of the butt coupling between Si-based laser and SiNOI chip. The inverse taper coupler (Section S3, Supporting Information), a conventional and widely used coupler, is fabricated as a comparison. The measured mode profiles of laser and three couplers are demonstrated in Figure 3c. The shape and dimensions of mode field of the two fork couplers are approximate to laser. Couplers with different tip widths are fabricated, and the measured results are presented in Figure 3d. The coupling loss between Si-based laser and fork1 coupler is measured as 1.175 and 1.265 dB for the fork2 coupler, which is ≈1 dB smaller than the inverse taper coupler (2.21 dB). It should be noted that in the measurement, a bare laser is used, which is easily damaged when the laser facet strikes the SiNOI chip facet, causing the reduction of power and distortion of mode field. Thus, the measured coupling losses are different from simulation results. The low coupling loss is conducive to improving the output power and decreasing power consumption of the whole photonics system. It is worthwhile mentioning that for the inverse taper coupler, due to the single tip, a much smaller tip width, 90 nm in layout (larger than the fabricated width) is necessary to expand mode profile, which is difficult to fabricate in most foundries.

To fully characterize the alignment tolerances between the Si-based laser and the edge couplers, we tune the x, y, z axes of the test stage until the minimal loss is obtained, and set this position as zero point. The zero-point position doesn't mean that the gap between laser chip and SiNOI chip is 0 µm. Then we shift the laser to measure the extra loss induced by different chip-to-chip coupling gaps, horizontal offset, and vertical offset, respectively. Figure 3e–g shows the measured alignment tolerances of fork1, fork2, and inverse taper couplers. For the gap between laser and Si_3N_4 couplers, the alignment tolerance with extra loss below 3 dB is 5.9, 6.7, and 2.9 µm for fork1, fork2, and inverse taper [Figure 3e]. The 3-dB alignment tolerance in the horizontal direction is from −3.8 µm to 3.6 µm, −3.3 µm to 2.7 µm, −2.9 µm to 2.9 µm [Figure 3f]. In the vertical direction, the extra 3-dB alignment tolerance is from −0.9 µm to 0.9 µm for two fork shape couplers, and −1.1 µm to 1 µm for inverse taper coupler [Figure 3g]. In addition to coupling loss, the alignment tolerances of the fork-shaped couplers are also superior to inverse taper couplers, especially in the gap.

Due to the divergence angle of the laser mode profile, when the gap between laser and SiNOI chip is increased, a larger mode field is captured by the Si_3N_4 coupler, causing the increscent coupling loss. When a deviation of alignment occurs in the

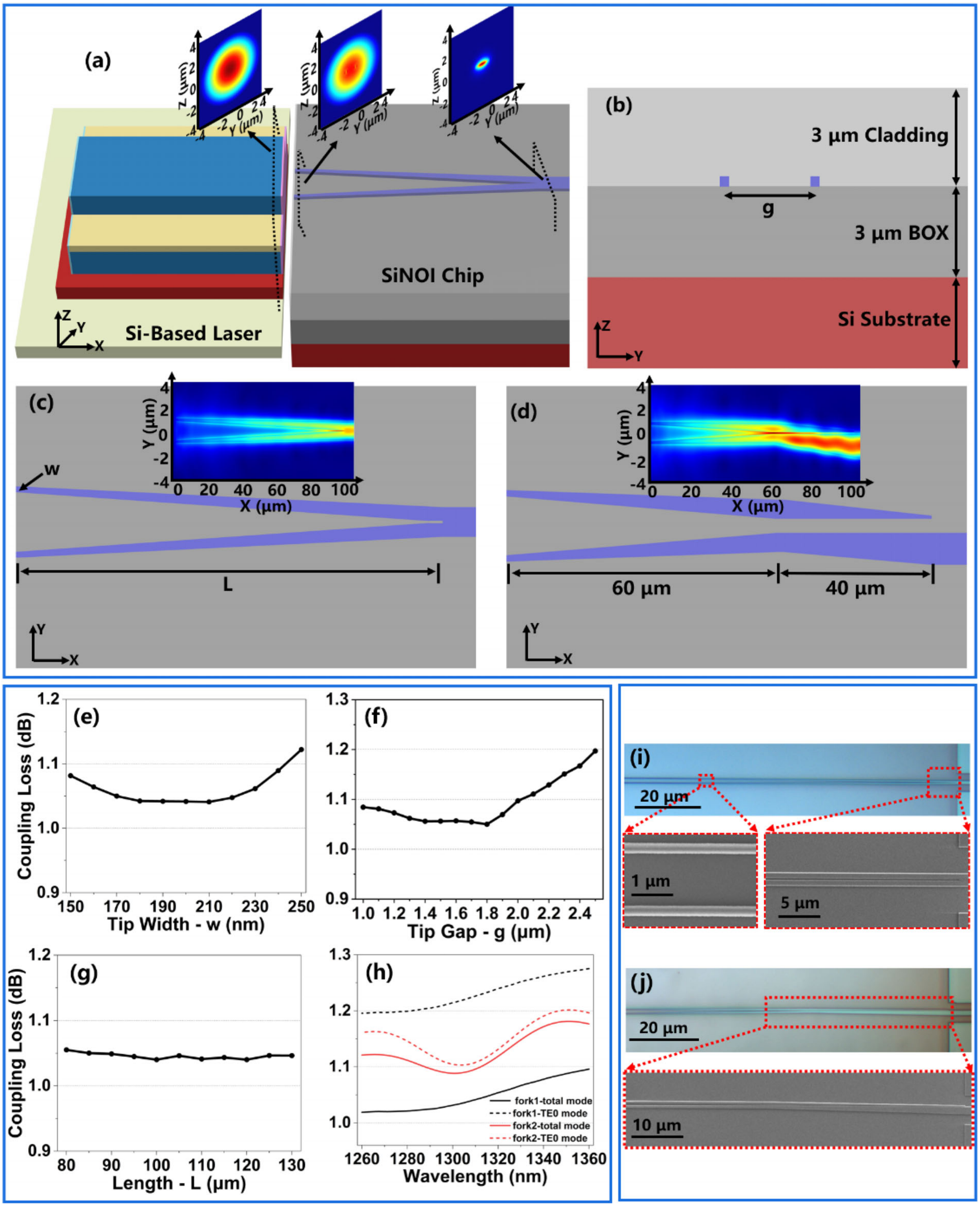

Figure 2. The proposed fork shape edge couplers. a–d) The schematic diagram of the edge couplers. a) Illustration of edge coupling strategy using fork1 shape coupler, and the mode transmission from Si-based III-V laser to SiN waveguide. b) Cross-sectional view of the SiNOI chip, the tip gap (g) between two Si_3N_4 tips is studied. c) The fork1 Si_3N_4 coupler, tip width (*w*), and coupler length (*L*) are studied in the design. d) The fork2 shape coupler, the optimization of different parameters is shown in Section S2 (Supporting Information). e–g) Simulation of the fabrication tolerance of the fork1 edge coupler. The coupling loss as a function of the e) tip width, f) tip gap, and g) coupler length. h) The coupling loss in the whole O band. The black solid and dashed lines denote the total mode and TE0 mode coupling loss of fork1 coupler, the red solid and dashed lines denote the total mode and TE0 mode coupling loss of fork2 coupler respectively. i,j) The fabricated couplers. Optical microscope image and SEM image of the i) fork1 and j) fork2 Si_3N_4 edge couplers.

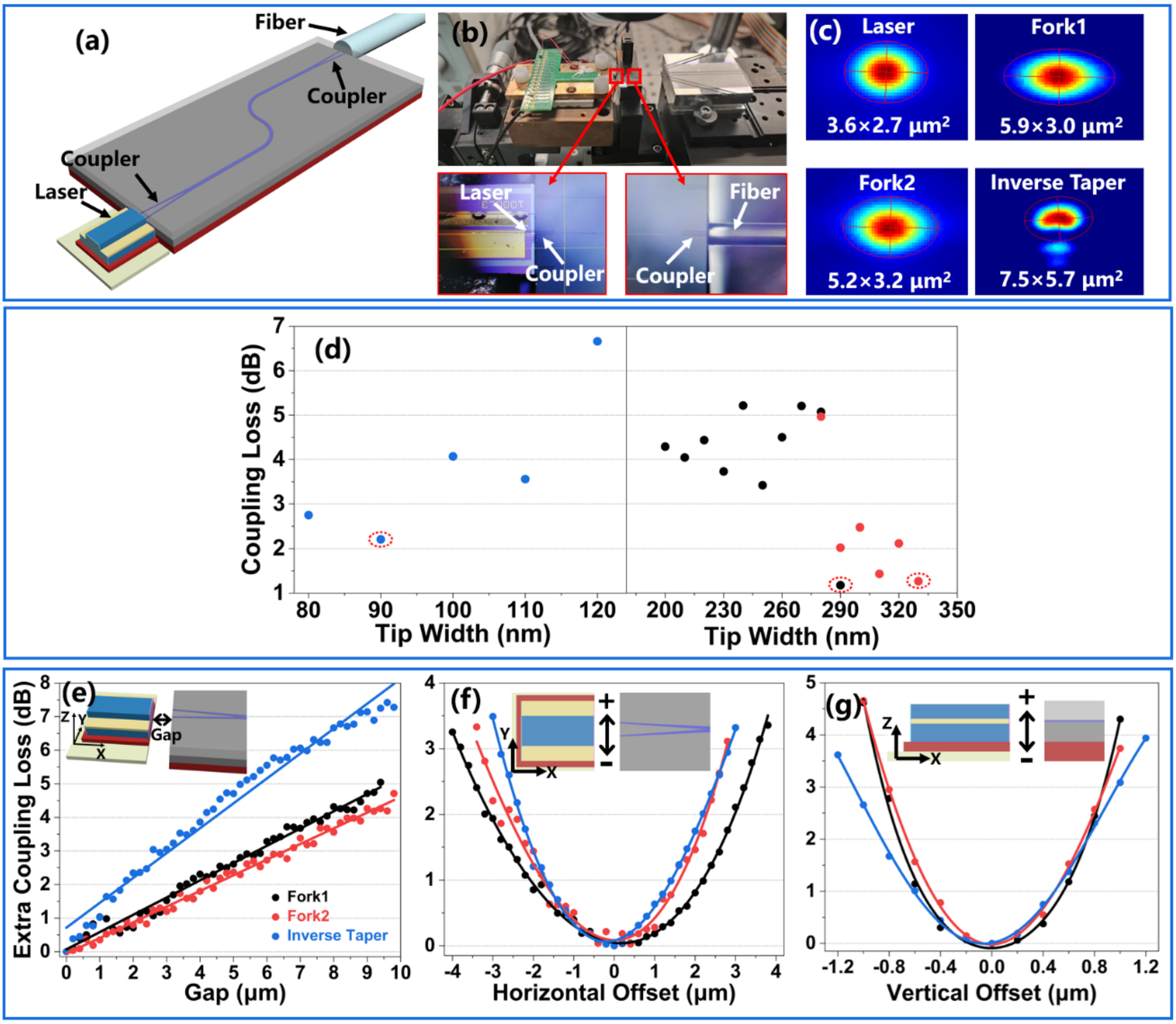

Figure 3. The measurement of the butt coupling between Si-based laser and SiNOI chip. a) The schematic diagram. b) The experiment platform. c) The measured mode profiles at the output facet of laser, fork1, fork2, and inverse taper coupler, respectively. d) The measured coupling loss of the fork1, fork2, and inverse taper edge couplers. The tip widths are the designed parameters on layout, which are larger than the fabricated parameters. The circled dots represent the minimum coupling losses. e–g) The measured alignment tolerance of the fork1, fork2, and inverse taper edge coupler. e) The extra coupling loss of different gaps between laser and SiNOI chip facet. f) The extra coupling loss of different horizontal offsets and g) vertical offsets. The dots represent the measured results, the lines represent the fit results.

horizontal or vertical direction, the coupler can only capture part of the incident light, more light diffuses into the surrounding silica, which also creates the extra loss. Furthermore, the thickness of the couplers is 200 nm, meaning the dimension in vertical direction is much smaller than horizontal direction. Hence the couplers show a better alignment tolerance in the horizontal direction. For the situation of SiNOI chip as the light source, such as light from Si_3N_4 waveguide to optical fiber or photodetector, the fork shape edge couplers also possess high efficiency and alignment tolerance.

The performance comparison of our proposed couplers and other reported couplers with various structures or materials is shown in **Table 1**. To the best of our knowledge, the fork couplers possess the minimum coupling loss. Our proposed fork-shaped edge couplers have greater pre-eminence in terms of coupling loss and tolerance, while the device compactness is not compromised. Particularly, the butt coupling strategies presented here provide an ease-of-fabrication and competitive solution for future full integration of light sources and various SiPh platforms.

5. Conclusion

In conclusion, we experimentally realize ultra-low loss butt coupling from Si-based InAs QD laser to Si_3N_4 waveguides with fork

Table 1. The performance comparison of the fork-shaped couplers and other reported couplers.

Reference	III-V Type	Coupler Platform	Coupler Structure	Coupler Length [μm]	Coupling Loss [dB]
This Work	Si-based QD Laser	Si_3N_4	Fork1	100	1.175
	Si-based QD Laser	Si_3N_4	Fork2	100	1.265
[47]	QW[a)] Laser	Si_3N_4	Taper	20	3.7
[48]	QW Laser	Si_3N_4	Taper with SiO_2 assistance	-[b)]	1.55
[49]	QW Laser	LN[c)]	Horn taper	-	5.2
[50]	QD Laser	SOI	Trident	150	3.9
[51]	Mid-IR laser	SOI	Suspended Taper	-	10

[a)] QW: Quantum Well; [b)] -: no data; [c)] LN: Lithium Niobate

shape couplers. The high-quality InAs/GaAs QD materials are directly grown on a Si substrate, and an ultra-low laser-to-chip coupling loss of only 1.175 dB is experimentally demonstrated with high alignment tolerance. The strategies presented in this paper provide a scalable and promising solution for the realization of either hybrid or monolithic integration between Si-based lasers and SiPh components. Employing our "embedded laser" scheme,[24] we believe that this monolithic epitaxy and ultra-low loss butt coupling techniques would realize the ambition toward high-density and large-scale SiPh integration, especially in the application fields such as on-chip optical interconnect and integrated lidar.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

A.H. and Y.C. contributed equally to this work. X.G. and T.W. conceived the idea and supervised the project. Y.S. provided assistance in the coordination of the project. A.H., J.X., and Y.C. designed the device parameters and the layout structure. A.H. and W.W. fabricated the device. A.H. and Y.C. performed the static measurement and data analyses. A.H., T.W., and X.G. wrote the paper. All the authors reviewed the paper and agreed on the contents. The authors also thank the Center for Advanced Electronic Materials and Devices (AEMD) of Shanghai Jiao Tong University (SJTU) for their support in device fabrication. This work was financially supported by the National Key R&D Program of China (2021YFB2800404) and the Natural Science Foundation of China (NSFC) (62175151 and 61835008).

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

edge couplers, hybrid integrations, Si-based lasers, silicon photonics

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